AN10920

Using CEC with TDA19989

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Document information

Info	Content
Keywords	HDMI, CEC internal clock calibration, CEC data registers, contiguous CEC read, write, message transfer
Abstract	This application note provides important advice to ensure that the Consumer Electronic Control (CEC) feature in the TDA19989 operates correctly

Revision history

Rev	Date	Description
01	20100419	Initial version

Contact information

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1. Introduction

The TDA19989 is a 150 MHz pixel rate HDMI 1.3a transmitter with 3 × 8-bit video inputs that includes an embedded feature which enables it to support the Consumer Electronic Control (CEC) protocol.

CEC operates over a bidirectional single-wire bus allowing communication of CEC-enabled AV products, connected by HDMI, over the home-appliance network using a single remote control.

This application note explains the exact requirements for the following functions that must be observed to ensure the TDA19989 CEC feature operates correctly:

- CEC internal clock calibration
- CEC data registers read/write

2. CEC internal clock calibration

The clock to the TDA19989 CEC module can be supplied either:

- externally from an external oscillator source

or

- internally from the TDA19989's dedicated internal Free Running Oscillator (FRO)

If the internal clock is used, it **must** be calibrated every time the TDA19989 is powered up.

The process for calibrating the internal clock is shown in the flow chart Figure 1. Note that it is imperative that the steps shown in the flow chart must be followed exactly to ensure that the internal clock is calibrated correctly.

Calibration functions controlled by the host processor are located in the software driver supplied with the TDA19989; for information on these functions you will need to refer to the *HDMI CEC User Manual*.

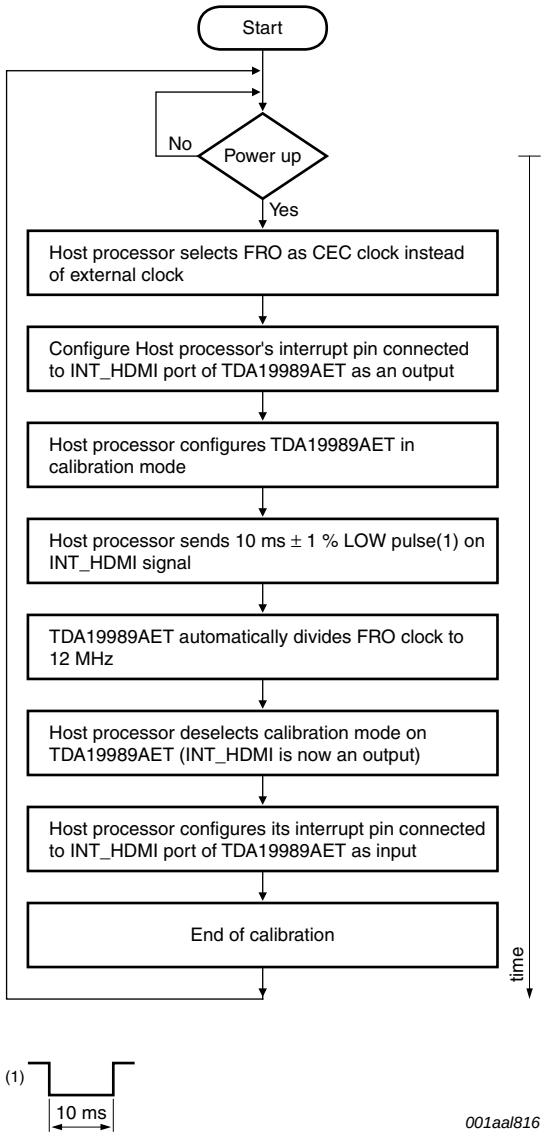


Fig 1. CEC internal clock calibration process

3. CEC data registers

CEC message data must be transferred contiguously and not in fragments. This requires the CEC data registers in the TDA19989 to be written or read in one communication sequence between a START bit and a STOP bit. The CEC data registers are located at addresses 07h to 19h.

Message transfers **must** always start from the first CEC data register CDR[0] at address 07h.

The maximum CEC message length supported is 16 bytes.

3.1 Writing to the CEC data registers

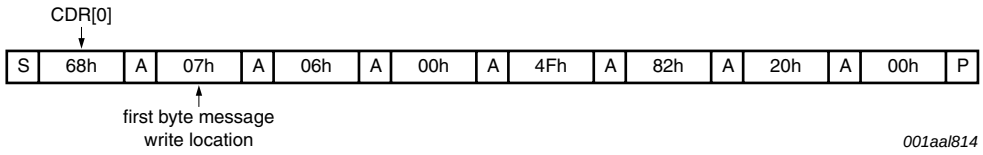
All CEC data write operations must start by addressing the first CEC data register CDR[0] at address 07h. CDR[0] indicates the number of CEC register bytes that are to be written to accommodate the complete message. These bytes are written contiguously.

The minimum CEC message length allowed is 3 CEC register bytes. Any message specifying less than 3 CEC register bytes is invalid.

If the number of CEC data registers actually written is less than the number indicated by CDR[0], the message is ignored and no acknowledge message is sent.

If the number of CEC data registers written is greater than the number indicated in CDR[0], the message is processed when the write to the last CEC data register specified in CDR[0] has completed. The extra message bytes are ignored.

If the message length indicated in CDR[0] exceeds the maximum number of CEC data registers available, the message is processed when the write to the last CEC data register has completed. The extra message bytes are ignored.



S = START bit.

A = Acknowledge bit.

P = STOP bit.

Fig 2. TDA19989 CEC data register write example

3.2 Reading the CEC data registers

All CEC data read operations must start by addressing the first CEC data register CDR[0] at address 07h. CDR[0] indicates the number of CEC register bytes that are to be read. These bytes will be read contiguously.

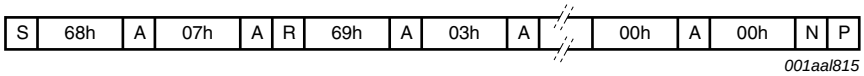
When the CEC data registers contain a valid message, line INT is set and the Status register INT bit is set to logic 1.

If the CEC data registers are read when line INT is not set, the value in CDR[0] is 0 which indicates there are no bytes to be read. Any further attempts to read before a STOP condition returns the value 00h.

If the host performs a write operation and then starts a read operation before resetting the Address Pointer register, the read operation starts automatically from CDR[0].

If the read operation stops before all of the specified CEC data registers are read, line INT is reset, the message is discarded and can never be read.

If the number of read CEC data registers is greater than the number indicated in the first CEC data register, the read value is 00h. Line INT is reset when the last valid CEC data register of the current message has been read.



S = START bit.

A = Acknowledge bit.

P = STOP bit.

R = Re-START bit.

Fig 3. TDA19989 CEC data register read example

4. Abbreviations

Table 1. Abbreviations

Acronym	Description
AV	Audio Visual
CEC	Consumer Electronic Control
HDMI	High Definition Multimedia Interface

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